

REMARKS

This is in response to the Office Action of May 19, 2004. With this response, claims 18 and 28 are amended. Consideration and favorable action of all pending claims 18-37 are respectfully requested.

In the Office Action, the Examiner rejected claims 18-20, 27-30 and 37 under 35 U.S.C. § 102(e) based upon Yamamoto. Further, claims 21 and 31 were rejected under 35 U.S.C. § 103 based upon Yamamoto in view of Sakamoto, claims 22, 23, 32 and 33 were rejected based upon Yamamoto in view of Lee et al. ('671) Claims 24-26 and 34-36 were rejected based upon Yamamoto in view of Lee ('652). It is believed that the claims as amended are patentably distinct from these references.

Independent claims 18 and 28 state that the electronic device under test is configured to operate using a constant voltage at a nominal power supply voltage. A power source supplies the constant power supply voltage at the nominal power supply voltage.

As discussed in the instant specification, some circuitry is designed to operate at nominal voltages. The present invention introduces disturbances which simulate unexpected deviations from these nominal voltages. The severity and frequency of such disturbances are highly random and can vary based upon a computer power supply capability, local utility quality, climate, operating environment, and other numerous factors. Design of circuitry, such as for disc storage products, must provide a certain amount of immunity to these disturbances for the products to survive and provide useful service throughout their life. The present invention provides a method and electronic device power testing apparatus in which a nominal voltage is applied to electronic components and disturbances are introduced into this nominal voltage to simulate the occurrence of such real world disturbances.

Independent claims 18 and 28 include providing power to an electronic device at a constant power supply voltage which is "at the nominal power supply voltage of the electronic device." Yamamoto does describe applying various voltage levels. However, the references do not appear to discuss application of the nominal supply voltage for the memory circuitry which is being tested. For this reason, the rejections should be withdrawn.

Additionally, amended claims 18 and 28 include the introduction disturbances which are, "configured to simulate an unexpected and random change in the nominal power supply voltage." As discussed in the instant application, such random disturbances can shorten the life expectancy of electronic devices. Yamamoto appears to show the application of a periodic (non-random) pulses to memory circuitry. However, the reference does not discuss unexpected and random changes in a nominal power supply voltage. For this additional reason, the rejection against the pending claims should be withdrawn.

Further, Applicant notes that the dependent claims contain numerous features which, when read in context with the independent claims, are not shown in the art. These combinations include introducing unexpected and random variations in a nominal power supply voltage in which a rising pulse having a maximum is controllable, a low going pulse having a minimum voltage, constant power supply voltage at 5 and 12 volt DC, the connection through an additional voltage connector, the additional voltage connector at 24 volts DC, a manually operated user interface to control the disturbances, at least one pulse having a duration and a magnitude which are controllable, a frequency of pulses which is controllable or a power-up sequence which is controllable.

In view of the above amendments and remarks, it is believed that the present application is in condition for

allowance. Consideration and favorable action are respectfully submitted.

The Director is authorized to charge any fee deficiency required by this paper or credit any overpayment to Deposit Account No. 23-1123.

Respectfully submitted,

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